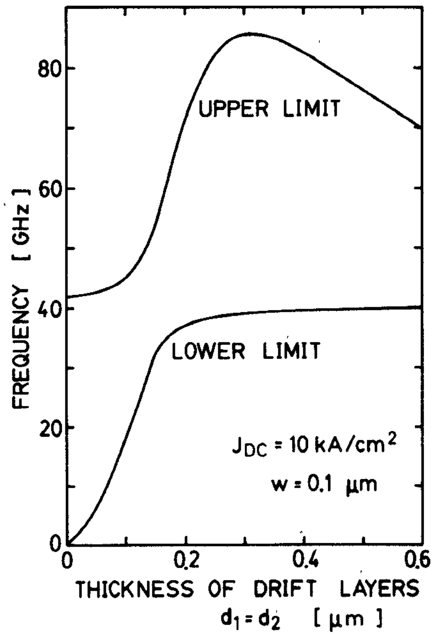

Fig. 5. Frequency range of amplification versus the drift-layer thickness.

μm, near the point where the avalanche resonance frequency of the avalanche layer [11] takes the highest value. Fig. 5 shows the frequency range of amplification against the drift-layer thickness with the avalanche-layer thickness kept constant. For the thicknesses below $d_1 = d_2 = 0.3$ μm, the upper frequency limit decreases with decreasing $d_1 = d_2$. This is because the relative amount of power dissipated in the inactive layers is larger for smaller active-layer thickness.

IV. Conclusions

We have presented a simplified field analysis of a distributed IMPATT diode in the traveling-wave mode using a multiple uniform layer approximation.

In order to understand thoroughly the operation of distributed IMPATT oscillators and amplifiers and to solve the problem of coupling these devices with other circuit components, the behavior of electromagnetic fields at the diode facets must be known. The IMPATT diode model presented in this paper will be useful for the analysis of these discontinuity problems.

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The authors wish to thank Y. Yamaguchi for his assistance in this work.

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The Effects of a Dielectric Capacitor Layer and Metallization on the Propagation Parameters of Coplanar Waveguide for MMIC

R. DELRUE, C. SEGUINOT, P. PRIBETICH, AND P. KENNIS

Abstract—**The study of coupling phenomena between lines laid on semiconductor substrates in MMIC technologies and the determination of propagation effects on power FET require the characterization lines with micron transversal widths. For such lines, the influence of metallization thickness and dielectric cap layer on propagation properties can no longer be neglected. The purpose of this paper is to characterize these effects for the case of coplanar lines laid on semiconductor substrates.**

I. Introduction

In the past, numerous lines laid on dielectric substrate have been studied, leading to the determination of the basic parameters (the attenuation and the phase constant) by means of various analytical and numerical techniques such as conformal mapping, finite element, finite difference, mode matching, and the spectral-domain approach. More recently, planar metal insulator semiconductor (MIS) or Schottky contact structures have been investigated by several authors [1]–[5] using the different kinds of numerical techniques.

In this paper we study the combined influence of thickness metallization and dielectric capacitor layer on the propagation parameters of coplanar lines on various semi-insulating or semiconductor substrates. The mathematical development used and the results which can be obtained by this numerical technique are presented.

II. Method

In order to take into account the most physical parameters and effects, we have studied the structures shown in Fig. 1(a) and (b) (a conductor-backed coplanar waveguide [1]) using the mode matching technique as in [3]. We consider the relative complex permittivity for each layer of the structure and the hybrid nature of the mode.

In this paper we focus our attention on the even dominant mode, so a magnetic wall is placed at $X = 0$, the symmetry axis of the structure.

The method used requires the division of the cross-sectional structure into subdomains in which the fields are expanded in a set of eigenfunctions relative to each subdomain (Fig. 1(c)). In

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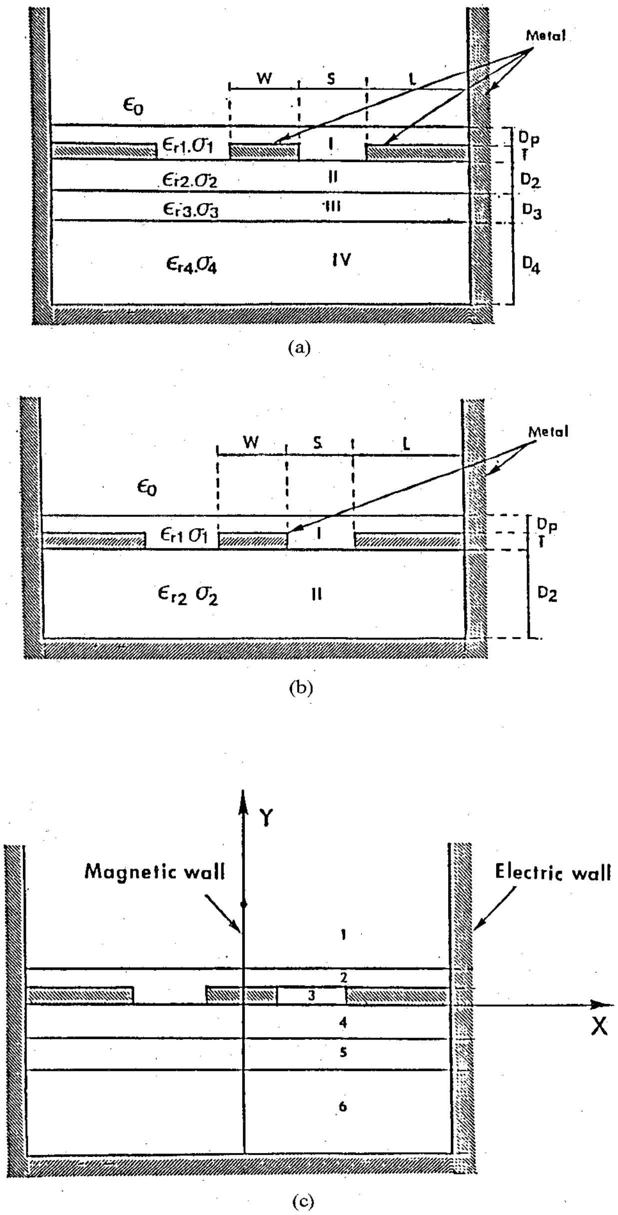

Fig. 1. (a) Studied structure. (b) Studied structure. (c) Division of the cross-sectional structure.

order to expand the fields, a hypothetical electric wall is placed as shown in Fig. 1(c). The behavior of the structure is only slightly perturbed when the electric wall is placed far away ($L = 100$ μm) from the slots of 1 μm width.

After determination of the field components in the different subdomains, the matching conditions at each interface lead to a set of homogeneous equations which can be written in matrix form as

$$Z * U = 0$$

where Z is a square matrix and U a vector which contains the unknown coefficient used for the different field expansions. The determinant of the matrix Z is set equal to zero to determine a nontrivial solution of the U vector, which at the same time leads to the complex propagation constant β. For each β value, the associated eigenvector U allows the complex time-averaged flow power P to be determined.

III. Results

For the structures studied in this paper the numerical convergence has been obtained by using nine terms of field expansion in the slot regions and 15 terms in other subdomains. This choice has been tested by comparisons of mode matching results for low thickness of metallization with the spectral-domain approach. We present in Figs. 2 and 3, for a frequency of 60 GHz, the variations of the relative effective permittivity and the characteristic impedance as a function of metallization thickness for the even dominant mode of a coplanar line laid on semi-insulating semiconductor substrate.

The characteristic impedance considered is

$$Z_{cv} = \frac{VV^*}{2P^*}$$

where V is the voltage in the slot (the asterisk signifies the complex conjugate values).

Two dielectric capacitor layers are considered, Si_3N_4 ($\epsilon_{r1} = 7.5$) and SiO_2 ($\epsilon_{r1} = 4.0$), both with the same thickness, $D_p = 1.0$ μm (Fig. 2(a)). We can observe that the relative effective permittivity decreases by 30 percent when the metallization increases from 0.1 μm to 1 μm without dielectric capacitor layer (Fig 2(a)). This variation is reduced when the Si_3N_4 or SiO_2 layer is taken into account.

Note that, naturally, the dielectric capacitor layer increases the relative effective permittivity. As shown in Fig. 2(b) and (c), the relative effective permittivity value is quite sensitive to a dielectric-filled gap between the metal strips, even without dielectric overlay over the coplanar line ($D_p = 0$). However the influence of the dielectric capacitor layer over the coplanar line is still very appreciable for the effective relative permittivity values ($D_p \neq 0$).

In the same way, Fig. 4 shows the combined influence of the metallization thickness and dielectric capacitor layer for coplanar lines laid on epitaxial doped substrates. In the study different thicknesses of dielectric capacitor layers have been considered, i.e., 0.1 μm and 2 μm for Si_3N_4 and SiO_2.

We can observe that the frequency behavior of the relative effective permittivity is strongly affected when a dielectric capacitor layer overlies a coplanar line laid on an epitaxial layer. For this kind of structure the fundamental hybrid mode is a slow wave mode, so the relative effective permittivity is greater than the permittivity of the substrate ($\epsilon_r = 13$). For this structure, Fig. 5 shows that the attenuation is not very sensitive to the presence of dielectric capacitor layer. Note that the tangent losses of this layer can be easily taken into account in the formulation of the problem. However, this effect can only be quite a small perturbation for lines laid on doped substrates compared to the bulk losses in the substrate.

Some remarks can be made concerning the variations of the relative effective permittivity. We must in fact differentiate between the absolute and the relative variations of relative effective permittivity. If we consider the absolute level, the effect of the dielectric capacitor layer is more important for a slow wave structure. In the case of the relative variation, the relative effective permittivity with and without a dielectric capacitor layer shows that its effect is more sensitive for lossless structure than for a slow wave one.

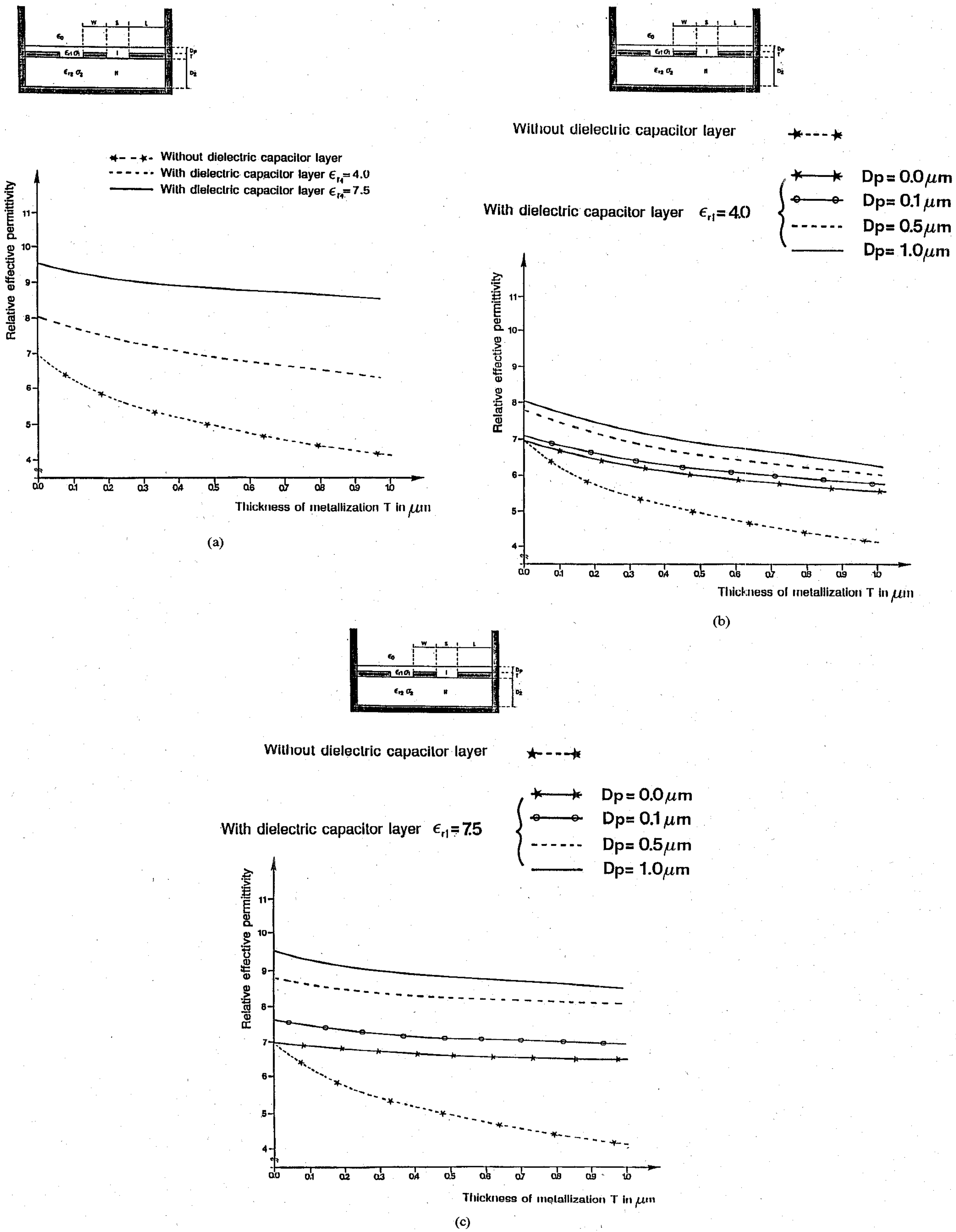

Fig. 2. (a) Evolution of the relative permittivity versus thickness of metallization and dielectric capacitor layer at $f = 60$ GHz for the structure in Fig. 1(b): $D_2 = 100$ μm; $W = S = 1.0$ μm; $\epsilon_{r2} = 13$; $D_p = 1.0$ μm; $\sigma_2 = \sigma_1 = 0$; $L = 100$ μm. (b) Evolution of the relative permittivity versus thickness of metallization and thickness of the dielectric capacitor layer at $f = 60$ GHz for the structure in Fig. 1(b): $D_2 = 100$ μm; $W = S = 1.0$ μm; $\epsilon_{r2} = 13$; $\sigma_2 = \sigma_1 = 0$; $L = 100$ μm. For $D_p = 0$, the gap between the metal strip is still filled with the dielectric. (c) Evolution of the relative permittivity versus thickness of metallization and thickness of the dielectric capacitor layer at $f = 60$ GHz for the structure in Fig. 1(b): $D_2 = 100$ μm; $W = S = 1.0$ μm; $\epsilon_{r2} = 13$; $\sigma_2 = \sigma_1 = 0$; $L = 100$ μm. For $D_p = 0$, the gap between the metal strip is still filled with the dielectric.

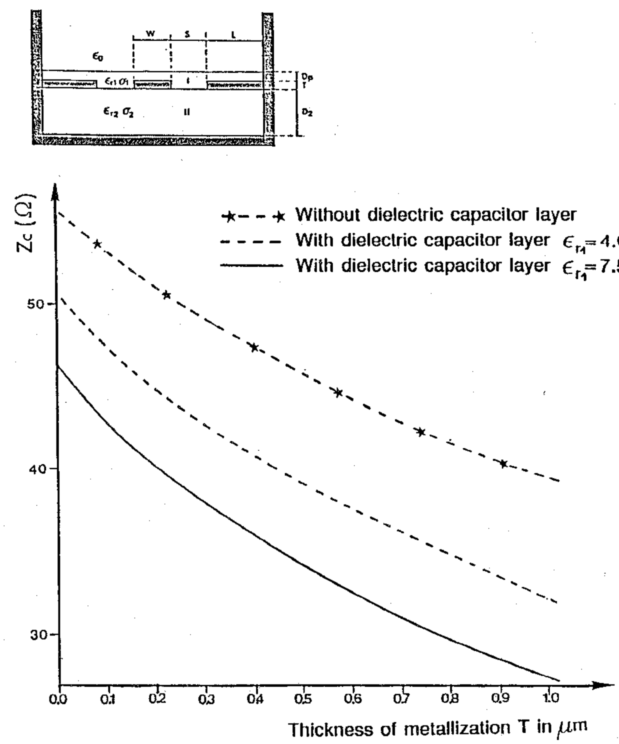

Fig. 3. Evolution of the characteristic impedance versus thickness of metallization and the dielectric capacitor layer at $f=60$ GHz for the structure in Fig. 1(b): $D_2=100$ μm; $D_p=1.0$ μm; $W=S=1$ μm; $\epsilon_{r2}=13$; $\sigma_2=0$; $\sigma_1=0$; $L=100$ μm.

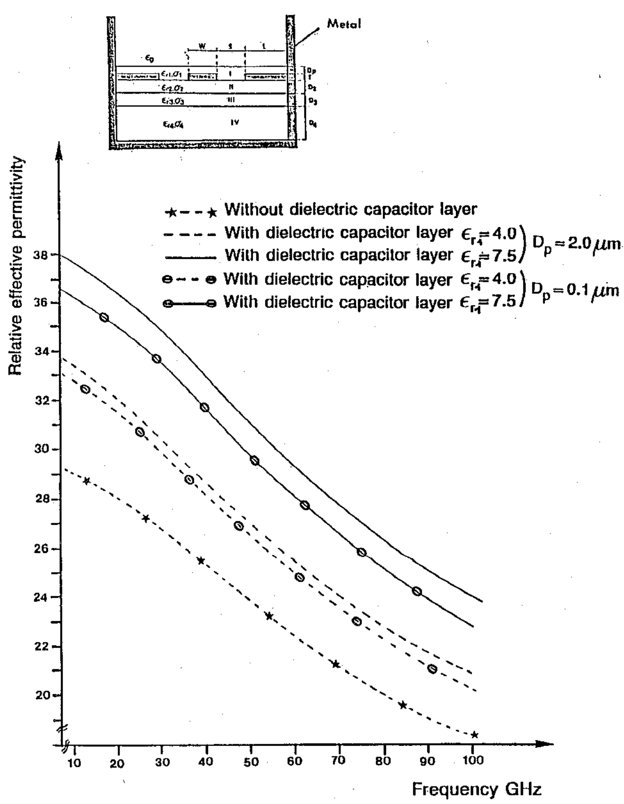

Fig. 4. Frequency behavior of the relative effective permittivity for the structure in Fig. 1(a): $T=0.1$ μm; $D_2=D_3=0.1$ μm; $D_4=100$ μm; $W=S=1$ μm; $L=100$ μm; $\epsilon_{r2}=\epsilon_{r3}=\epsilon_{r4}=13$; $\sigma_1=\sigma_2=0$; $\sigma_3=106$ mho/cm; $\sigma_4=1\cdot e^{-7}$ mho/cm.

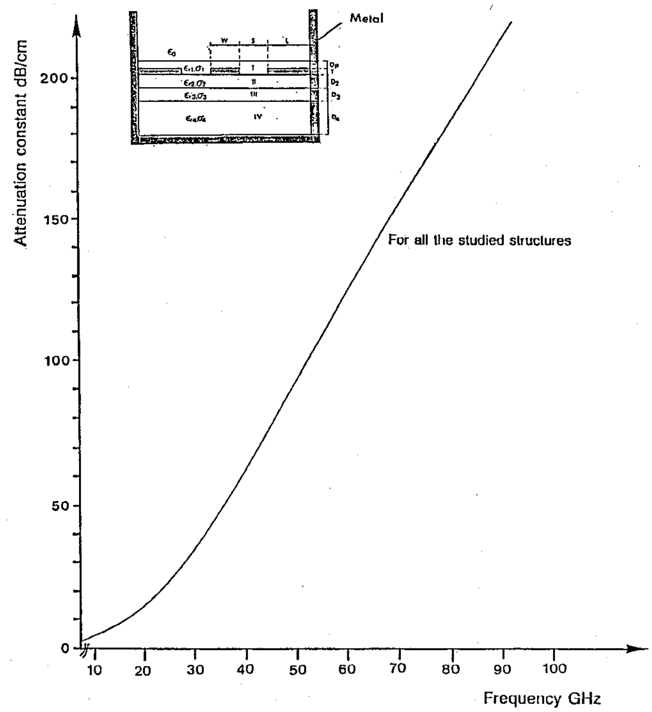

Fig. 5. Frequency behavior of the attenuation for the structure in Fig. 1(a): $T=0.1$ μm; $D_2=D_3=0.1$ μm; $D_4=100$ μm; $W=S=1$ μm; $L=100$ μm; $\epsilon_{r2}=\epsilon_{r3}=\epsilon_{r4}=13$; $\sigma_1=\sigma_2=0$; $\sigma_3=106$ mho/cm; $\sigma_4=1\cdot e^{-7}$ mho/cm.

IV. Conclusions

This paper contributes to the understanding of the frequency behavior of realistic coplanar lines with micron transversal dimensions laid on semiconductors and semi-insulator substrates for MMIC applications.

It points out the simultaneous effects of a dielectric capacitor layer and the thickness of metallization on the propagation characteristics of such lines. This study allows us to quantify the variations of relative effective permittivity due to the presence of a dielectric capacitor layer. For the most usual passivation overlay used in MMIC's, that is, Si_3N_4 and SiO_2, the relative effective permittivity decreases about:

- 30 percent without dielectric capacitor layer
- 20 percent for a dielectric capacitor layer SiO_2 ($\epsilon_r=4.0$)
- 10 percent for a dielectric capacitor layer Si_3N_4 ($\epsilon_r=7.5$)

when metallization increases from 0.1 μm to 1 μm for a dielectric capacitor layer of 1 μm thickness.

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